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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,038	12/11/2003	Theodore W. Houston	TI-35881	8454
23494 7590 05/09/2007 TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			EXAMINER LE, THONG QUOC	
			ART UNIT 2827	PAPER NUMBER
			MAIL DATE 05/09/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/733,038

Applicant(s)

HOUSTON, THEODORE W.

Examiner

Thong Q. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,5,6,8-10,12-17 and 19-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,5-6,8-10,12-17,19-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Amendment filed on 03/16/2007 has been entered.
2. Claims 1,5-6,8-10,12-17,19-21 are presented for examination.

***Continued Examination Under 37 CFR 1.114***

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/16/2007 has been entered.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,5-6,8-10,12-17,19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Shyu (U.S. Patent No. 6,046,957).

Regarding claims 1, 12, Shyu discloses an SRAM device (Figure 7), comprising:  
an SRAM array (Figure 7, 20) coupled to row peripheral circuitry (Figure 7, 21)  
by a word line (Figure 7,256) and coupled to column peripheral circuitry (Figure 7, 220,  
222, 22) by bit lines (Figure 7, 16) ; and

an array low voltage control circuitry (Figure 5, 122) that provides an enhanced low operating voltage  $V_{ESS}$  to said SRAM array during at least a portion of a READ operation or a WRITE operation thereof (Column 2, lines 57-65), said enhanced low operating voltage  $V_{ESS}$  having a higher value than a low operating voltage  $V_{SS}$ , and wherein said array low voltage control circuitry provides said enhanced low operating voltage  $V_{ESS}$  at a lower value during said READ operation than during said WRITE operation (Column 2, lines 56-67, Column 3, lines 1-5,  $V_{pp}$  higher than  $V_{CC}$ ).

Regarding claims 5, 16, Shyu discloses wherein array low voltage control circuitry provides said enhanced low operating voltage  $V_{ESS}$  based on a factor selected from the group consisting of: a process corner, a transistor parameter, a mode of operation (Column 2, lines 60-65, Figure 7, MIN, Column 5, lines 8-20), and a value of a high supply voltage.

Regarding claims 6, 17, Shyu discloses wherein said array low voltage control circuitry provides said enhanced low operating voltage  $V_{ESS}$  at a higher value when based on a strong n process corner (Column 3, lines 1-5).

Regarding claims 8, 19, Shyu discloses wherein said array low voltage control circuitry only provides said lower value for an addressed column of said SRAM array (Figure 7, 23, Column 5, lines 60-67, Column 6, lines 1-15).

Regarding claims 9, 20, Shyu discloses wherein said array low voltage control circuitry employs an active component to provide said enhanced low operating voltage  $V_{ESS}$  (Column 2, lines 40-65).

Regarding claims 10, 21, Shyu discloses wherein said array low voltage control circuitry provides said enhanced low operating voltage V<sub>ESS</sub> employing a component selected from the group consisting of: a diode, a transistor, a fuse, a ROM, a voltage regulator, and logic circuitry (Figure 9, 27).

Regarding claims 13-15, Shyu discloses wherein said providing only occurs during a WRITE operation (Column 2, lines 62-65), and wherein said providing occurs during all of said active mode (Column 3, lines 1-5), and wherein said providing occurs during all modes (Column 3, lines 1-5).

6. Claims 1,12 are rejected under 35 U.S.C. 102(b) as being anticipated by Devanney (U.S. Patent No. 5,541,883).

Regarding claim 1, 12, Devanney discloses an SRAM device (Figure 1) , comprising: an SRAM array (Figure 1) coupled to row peripheral circuitry (Figure 1, ) by a word line (Figure 1, 110) and coupled to column peripheral circuitry by bit lines (Figure 1, BIT) ; and an array low voltage control circuitry that provides an enhanced low operating voltage V<sub>ESS</sub> to said SRAM array during at least a portion of a READ operation or a WRITE operation thereof, said enhanced low operating voltage V<sub>ESS</sub> having a higher value than a low operating voltage V<sub>SS</sub>, and wherein said array low voltage control circuitry provides said enhanced low operating voltage V<sub>ESS</sub> at a lower value during said READ operation than during said WRITE operation (Column 3, lines 20-27).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Thong Q. Le  
Primary Examiner  
Art Unit 2827